REMARKS

Claims 1-8, 10-14, 16 and 17 have been presented for examination in the Patent U.S. Patent Application.

Claims 1-8, 10-14, 16 and 17 have been rejected in the Office Action dated November 16, 2006, this rejection having been made final.

In this Continuation Application, Claim 6, 8, and 12 have been cancelled, Claims 9, and 15 having been previously cancelled.

Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 are in the Continuing Application and reconsideration of the Continuing Application is hereby respectfully requested.

Referring to Paragraph 1 of the Office Action date November 16, 2006, Claims 1-3, 7, 8, 10, 14, and 16 have been rejected under 35 U.S.C. 103(a) as obvious over U.S. Patent 6,732,2061 issued in the name of Jensen et al (herein after referred to as Jensen) in view of U.S. Patent 5,870,628 issued in the name of Chen et al (hereinafter referred to as Chen). Claims 5, 6, 9, 13, and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Jensen, cited above, in view of Chen cited above, in further view of U.S. Patent 6,029,212 issued in the name of Kessler et al (hereinafter referred to as Kessler).

Before addressing the relationship of the references to the invention sought to be protected by the Claims, the invention defined by the Claims in the Application will be discussed. The present invention includes an interface unit for the ATM slave processing unit. This description implies that there is an ATM

master processor unit that is part of the complete system. The signals exchanged between the ATM master processor unit and the ATM slave processor unit are shown in the Figures of the Application. The ATM slave processor interface unit must therefore be designed to accommodate this signal exchange. In particular, to minimize the apparatus required, a two-stage FIFO is used both in the input section of the ATM slave processor interface unit and in the output section of the ATM slave processor interface unit. Notice that the two-stage input unit is possible because of the difference in the clock times of the bus coupling the ATM master processor and the ATM slave processor. The interface unit in the ATM slave processor and in the ATM master processor receives from or transmits to the bus signals at a relatively slow rate. In exchanging the signals from two-stage FIFO register to the remainder of the ATM processor, the processor operated as a sufficient clock rate relative to the bus clock rate that the two-stage FIFO register can be filled or emptied by the ATM processor immediately relative to the interaction with the bus.

Referring first to Jensen and the Chen references as related to Claims 1, 10, and 14, the independent Claims of the Application, neither these references nor the reference of Kessler, disclose the interaction of an ATM slave processor unit with an ATM master processor unit using the UTOPIA signal format. In contradistinction, the signals exchanged between the ATM master processor unit and the ATM slave processor unit using the UTOPIA protocol is specifically described. The references do not disclose or claim an interface unit that includes both an input section and an output section. Consequently, it is believed that Claims 1, 10, and 14 are patentably distinct from the Jensen, Chen and Kessler reference.

The independent Claims or the dependent Claims dependent from the independent Claims 1, 10, and 14 further include the limitation of a two-stage FIFO in the input section and in the output section of the interface unit. In view of this difference, the Claims including this limitation are patentably distinct from the references.

Referring specifically to the Jensen reference, this reference includes a FIFO input register. However, as seen by Fig. 1, this reference does not include a direct memory access unit. In the Chen reference, a direct memory access unit is shown, but the reference includes a plurality of FIFO unit. It is not clear how, without the benefit of the teaching of the present Application, these references can be combined. Therefore, rejection of the Claims of the present Application over Jensen in combination with Chen is respectfully traversed.

Dependent Claims of the present application further include the limitation of the transfer of signal groups for each clock cycle in a two-stage FIFO register. As indicated above, the present invention recognizes that this can be accomplished with both the input interface section and the output interface section because of the difference in the clock rates between the system bus and the direct memory access unit. This limitation is patentably distinct from the disclosure teaching and claims of the Jensen, Chen, and Kessler references.

Claims 2-5, 7, 11, 13, 16 and 17 all depend from either Claim 1, Claim 10, or Claim 14, the independent Claims of the Application. Therefore dependent Claims 2-5, 7, 11, 13, 16 and 17 are patentable for the same reasons that Claim 1, 10, and 14 are patentable.

Therefore, rejection of Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 under 35 U.S.C. 103(a) over by reference to Jensen, in view of Chen, in further view of Kessler is respectfully traversed.

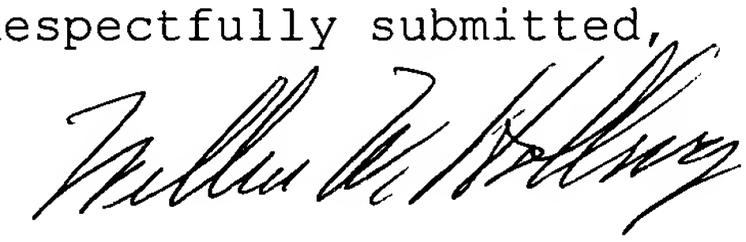
CONCLUSIONS

In view of the foregoing amendments and the foregoing discussion, it is believed that Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 are now in condition for allowance and allowance of Claims 1-5, 7, 10, 11, 13, 14, 16 and 17 is respectfully requested.

Should any issues remain that can be addressed by telephone interview, Examiner is respectfully requested to call the undersigned attorney at 281-274-4064.

Please charge any fees in connection with the filing of this amendment, including extension of time fees if any, to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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